PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 on April 18, 2003.

Stephanie Daryaie

Stephanie Daryaie

Applicant	:	Jan S. Iwanczyk, et al.
Application No.	:	09/835,937
Filed	:	April 16, 2001
Title	:	JUNCTION-SIDE ILLUMINATED SILICON DETECTOR ARRAYS
Grp./Div.	:	2878
Examiner	:	Constantine Hannaher
Docket No.	:	41876/RAG/P590

AMENDMENT

Post Office Box 7068
Pasadena, CA 91109-7068

Assistant Commissioner for Patents
Washington, D.C. 20231

April 18, 2003

Commissioner:

In response to the Office action of December 18, 2002, please amend the above-identified application as follows:

In the Specification:

On page 2, lines 8-19, please replace with the following paragraphs:

Other broad applications including radiation hardened detector arrays for high-energy physics research would also benefit from a development of low cost, high-yield detector array structures.

Typical silicon photodiode arrays with parallel signal readout are based on (p+)-(n)-(n+) structures constructed on high resistivity (1 - 100 ohm-m) silicon wafers. P+ contacts forming junctions in the n-type substrate are constructed in the form of a diode array. A